

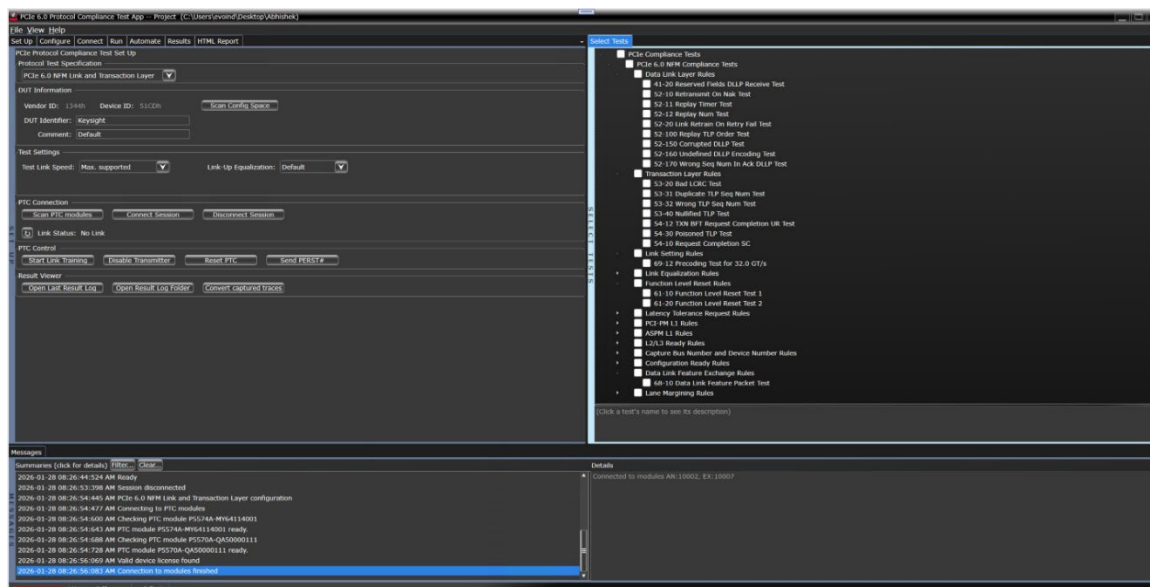
P5578CTSA PCIe 6.0 Protocol Compliance Test Suite

PCI Express® 6.0

Introduction

PCI Express® (PCIe®) protocol compliance testing verifies that a Device Under Test (DUT) adheres to the behavioral, architectural, and protocol requirements defined by the PCIe Link and Transaction Layer specifications. These specifications are governed and released by the PCI-SIG®, ensuring global interoperability, reliability, and consistency across PCIe-compatible components.

The **P5578CTSA PCIe 6.0 Protocol Compliance Test Suite** enables complete automation of PCIe 6.0 link and transaction layer compliance testing. By executing standardized test cases under controlled stress conditions, the suite helps hardware designers, validation teams, and compliance labs ensure DUT readiness for real-world deployment and PCI-SIG compliance workshops.



Product Overview

PCIe 6.0 introduces significant architectural advancements, including **FLIT (Flow Control Unit) encoding**, supporting 64 GT/s data rates and enhanced efficiency. The P5578CTSA software enables comprehensive testing of PCIe 6.0 devices across both FLIT and non-FLIT operational modes.

The compliance test suite:

- Executes **all mandatory link and transaction layer compliance tests** for PCIe 6.0.
- Provides **fully automated test execution**, reporting, and result analysis.
- Supports **PCIe 6.0 FLIT mode (46 tests)** and **non-FLIT mode (45 tests)**.
- Maintains **backward compatibility with PCIe 5.0**, including PCIe 5.0 link, transaction, and retimer test cases.

This ensures continuity for legacy hardware validation while enabling seamless adoption of PCIe 6.0 technologies.

Test Selection and Configuration

Upon launch, the software presents a configuration dialog allowing users to select the desired test categories:

- PCIe 6.0 FLIT Mode Compliance Tests (mandatory for 64 GT/s)
- PCIe 6.0 Non-FLIT Mode Compliance Tests
- PCIe 5.0 Link & Transaction Tests
- PCIe 5.0 Retimer Tests

Note: FLIT mode supports lower PCIe data rates but is applicable *only* to PCIe 6.0 devices. Earlier PCIe generations do not support FLIT functionality.

This is shown in the figures 1, 2 and 3 below.

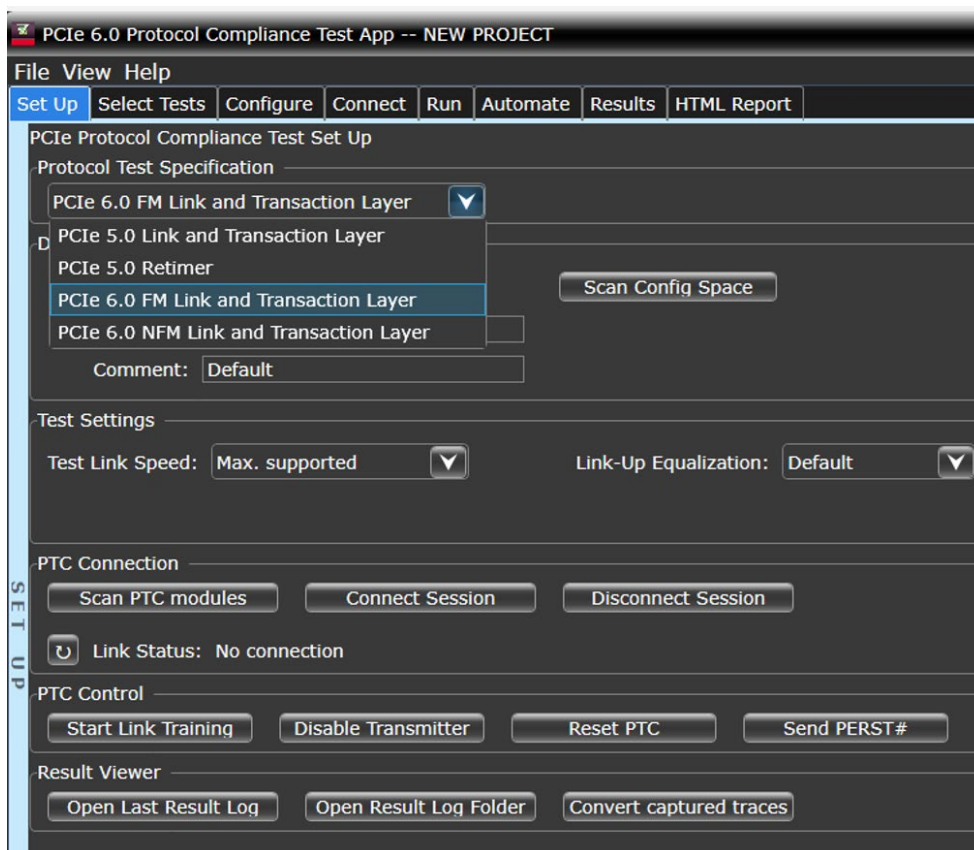


Figure 1. Selection of test specification

Graphical User Interface (GUI) Overview

The **P5578CTSA PCIe® 6.0 Protocol Compliance Test Suite** features a streamlined and intuitive user interface designed to simplify configuration, execution, and analysis of PCIe 6.0 compliance testing.

User Interface and Navigation

The software provides an **easy setup navigation menu** (figure 2), enabling rapid configuration of PCIe 6.0 link-up parameters and selection of link and transaction layer compliance test cases.

- A **real-time status panel** at the lower-left corner (figure 3) displays continuous progress updates, including step-level execution details for each test case.
- A **test case selection panel** on the right-hand side (figures 4 and 5) offers categorized groups of:
 - **PCIe 6.0 test cases**
 - **Non-FLIT Mode (NFM) test cases**
 - **FLIT Mode (FM) test cases**

This structured layout ensures clear visibility and quick navigation through all required compliance tests.

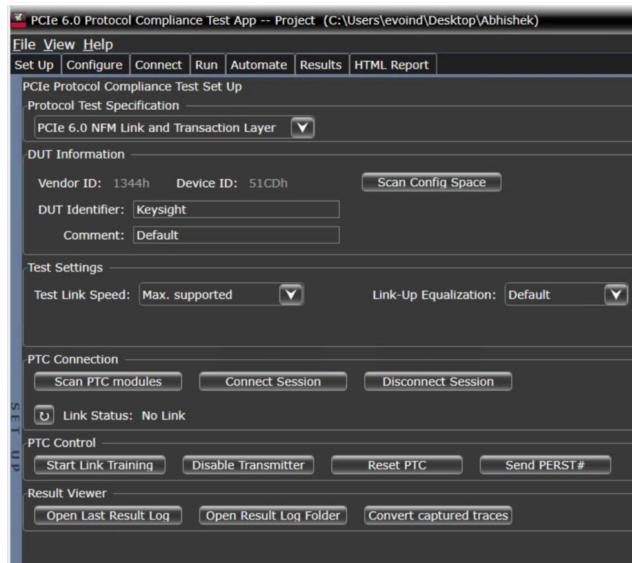


Figure 2. Easy setup navigation menu.

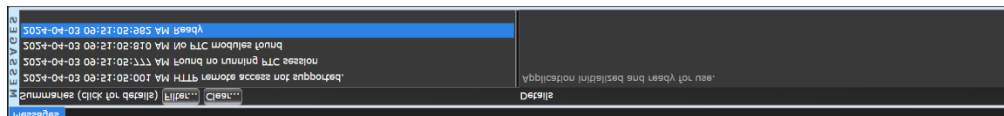


Figure 3. Monitor status details of each test.

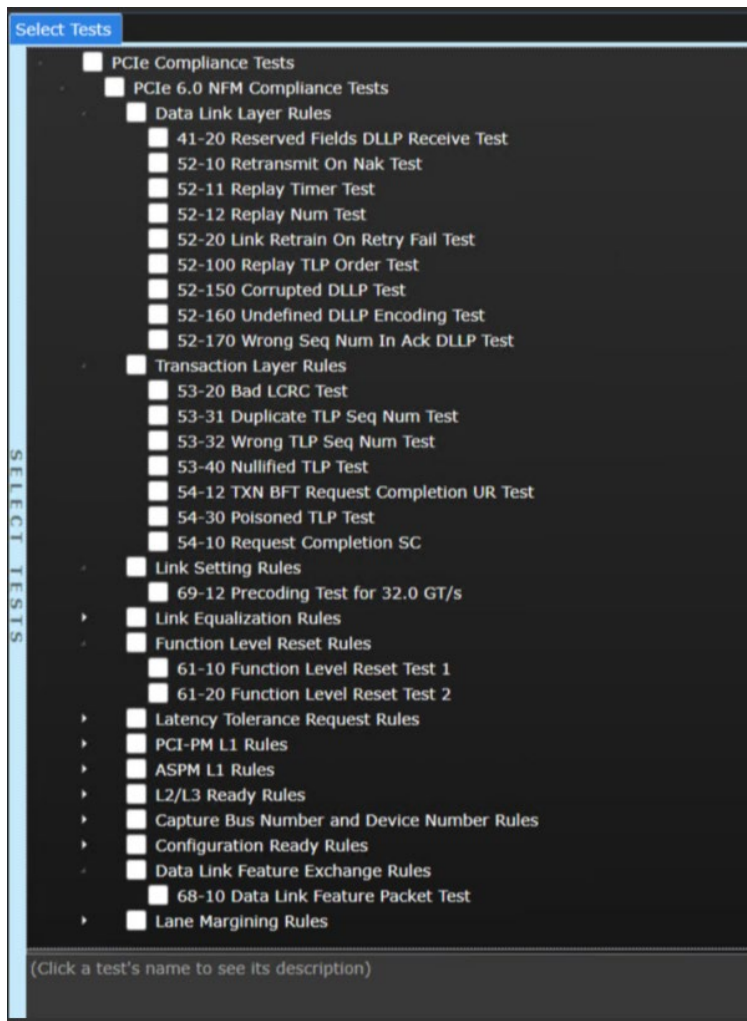


Figure 4. List of test cases: NFM compliance tests

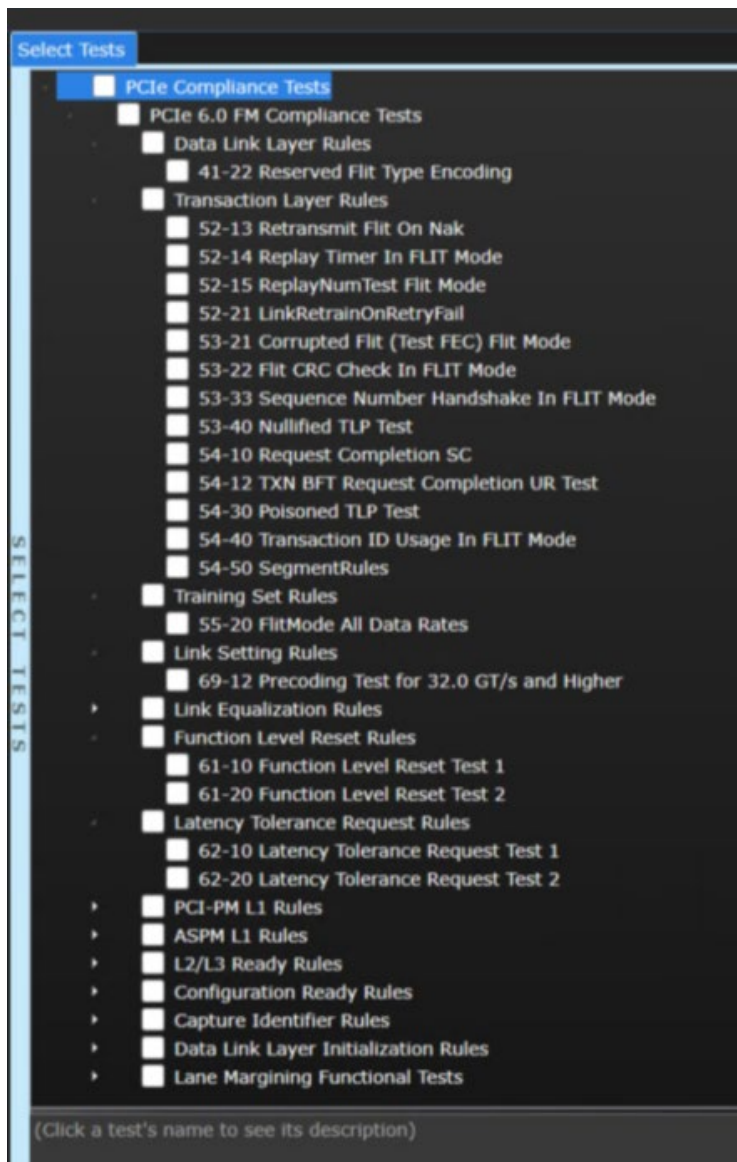


Figure 5. List of test cases: FM compliance tests

Flexible and Automated Test Execution

The GUI provides users with full control over test execution:

- Selection of **individual test cases** or complete test groups.
- Ability to run selected tests **once** or for **multiple iterations**, supporting stress and regression testing (figure 6).
- Support for **script-based customization**, enabling advanced users to modify or automate sequences for specialized workflows (figure 7).

Instant Results and Detailed Reporting

During execution, test outcomes are updated **instantly** in the results panel (figure 8), allowing engineers to monitor DUT behavior in real time.

After completion, the software generates a **comprehensive compliance report** summarizing:

- Number of executed tests
- Individual **pass/fail** outcomes
- Additional diagnostic details for debugging and certification preparation

This provides a complete documentation package suitable for internal validation and PCI-SIG® compliance readiness. This is shown in figure 9 below.



Figure 6. Easy automated one-push “Run” button.

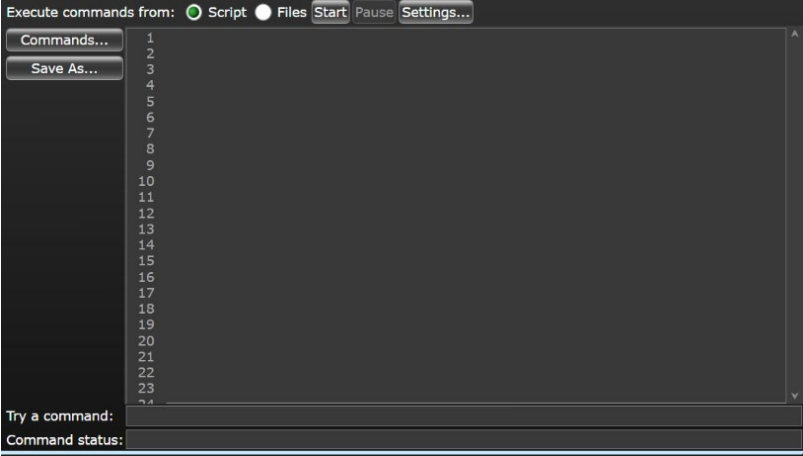


Figure 7. Customizing tests using sripts.

Test Name	Actual Value	Margin %	Pass Limits	# Trials
41-20 Reserved Fields DLLP Receive Test	Pass	100.000	VALUE = 1 1	
52-10 Retransmit On Nak Test	Pass	100.000	VALUE = 1 1	
52-11 Replay Timer Test	Pass	100.000	VALUE = 1 1	
52-12 Replay Num Test	Pass	100.000	VALUE = 1 1	
52-20 Link Retrain On Retry Fail Test	Pass	100.000	VALUE = 1 1	
52-150 Corrupted DLLP Test	Pass	100.000	VALUE = 1 1	
52-160 Undefined DLLP Encoding Test	Pass	100.000	VALUE = 1 1	
52-170 Wrong Seq Num In Ack DLLP Test	Pass	100.000	VALUE = 1 1	
53-20 Bad LCRC Test	Pass	100.000	VALUE = 1 1	
53-31 Duplicate TLP Seq Num Test	Pass	100.000	VALUE = 1 1	

RESULTS

Parameter	Value
59-10_TestResult	Pass

SELECT TESTS

Figure 8. View instant results.

KEYSIGHT

Test Report

PASS

Test Configuration Details

Application

Name

Version

Device Description

Spec

TestSpeed

Equalization

Test Session Details

Debug Mode Used

Compliance Limits

Last Test Date

Summary of Results

Test Statistics

Failed: 0

Passed: 15

Incomplete: 0

Total: 15

Margin Thresholds

Figure 9. View and generate test report

Typical Test Setup & Hardware Requirements

The P5578CTSA software controls the full PCIe 6.0 protocol test configuration consisting of:

- A **PCIe 6.0 Protocol Exerciser** (P5573A / P5574A / P5575A)
- A **PCIe 6.0 Protocol Analyzer** (P5570A / P5571A / P5572A)
- A **PCIe 6.0 Test System (Backplane)** (P5563C)
- **The DUT (e.g., PCIe add-in card)**

All analyzer and exerciser lane-width variants (**x1, x4, x8, x16**) are fully compatible with P5578CTSA. For PCIe 6.0 protocol testing, an **x1 link width** is sufficient.



Figure 10. Typical PCIe 6.0 protocol solution test setup

Ordering Information

Model	Description	Comments
P5578CTSA	PCIe 6.0 Protocol Compliance Test Suite	
P5573A, P5574A or P5575A	PCIe 6.0 Exerciser with Linkwidth x16, x8 or x4 respectively	
P5577PSWA	PCIe 6.0 Exerciser Software	Optional
P5570A, P5571A or P5572A	PCIe 6.0 Analyzer Linkwidth x16, x8 or x4 respectively	
P5576PSWA	PCIe 6.0 Analyzer Software	Optional
R-55A-001-3	KeysightCare Assured - Extend to 3 years	
P5563C	PCIe 6.0 Test System (Backplane)	

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